

Inventor: John T. Moore  
Title: Methods of Forming Dielectric Materials and Methods of Processing  
Semiconductor Substrates  
Assignee: Micron Technology, Inc.

**INFORMATION DISCLOSURE STATEMENT**  
**PURSUANT TO 37 C.F.R. §§ 1.56, 1.97 AND 1.98**

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a continuation application of co-pending application Serial No. 09/602,381, filed June 22, 2000. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2).

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: November 3, 2003

By: Jennifer J. Taylor  
Jennifer J. Taylor, Ph.D.  
Reg. No. 48,711

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			ATTY. DOCKET NO. M122-2438	SERIAL NO. PRIORITY 09/602,381	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)					APPLICANT Micron Technology, Inc.		
					FILING DATE PRIORITY June 22, 2000	GROUP PRIORITY 2815	
U.S. PATENT DOCUMENTS							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
AA	5,032,545	07-1991	Doan et al.				
AB	5,436,481	07-1995	Egawa et al.				
AC	5,378,645	01-1995	Inoue et al.				
AD	5,258,333	11-1993	Shappir et al.				
AE	5,518,946	05-1996	Kuroda				
AF	5,445,999	08-1995	Thakur et al.				
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AI	5,026,574	06-1991	Economu et al.				
AJ	5,612,558	03-1997	Harshfield				
AK	5,719,083	02-1998	Komatsu				
AL	5,760,475	06-1998	Cronin				
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						Yes	No
AM	WO 96/39713	12-1996	PCT				
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
AR		Wolf, S., "Silicon Processing for the VLSI Era", Lattice Press 1990, Vol. 2, pp. 212-213.					
AS		Wolf, S., "Silicon Processing for the VLSI Era", Lattice Press 1990, Vol. 2, pp. 188-189, 194-195, 609-614.					
AT		Ko, L. et al., "The Effect of Nitrogen Incorporation into the Gate Oxide by Using Shallow Implantation of Nitrogen and Drive-In Process", IEEE 1996, pp. 32-35.					
EXAMINER				DATE CONSIDERED			
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>							

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AB	5,619,057	04-1997	Komatsu				
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AE	6,174,821	01-2001	Doan				
AF	5,939,750	08-1999	Early				
AG	5,254,489	10-1993	Nakata				
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	Kuroi, T. et al., "The Effects of Nitrogen Implantation Into P+Poly-Silicon Gate on Gate Oxide Properties", 1994 Sympos. on VLSI Technology Digest of Technical Papers, IEEE 1994, pp. 107-108.						
AT	Liu, C.T. et al., "Multiple Gate Oxide Thickness for 2GHz System-on-a-Chip Technologies", IEEE 1998, pp. 589-592.						
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	AF	6,114,203	09-2000	Ghidini et al.				
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	AJ	6,140,187	10-2000	DeBusk et al.				
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	AA	5,763,922	06-1998	Chau				
	AB	6,225,167 B1	05-2001	Yu et al.				
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	AA	6,331,492 B2	12-2001	Misium et al.				
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	AF	6,184,110 B1	02-2001	Ono et al.				
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	AF	5,840,610	11-1998	Gilmer et al.				
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	AI	6,482,690 B2	11-2002	Shibata				
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